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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/760,359	01/21/2004	Yoshihiro Saeki	030712-21	8709

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NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
HA, NATHAN W	
ART UNIT	**PAPER NUMBER**
2814	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/760,359	SAEKI ET AL.	
	Examiner	Art Unit	
	Nathan W. Ha	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

a. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the limitation, "low noise resistivity circuit includes an analog circuit", must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohie (US 6,580,164, newly cited) and in view of Gutierrez (US 6,879,023, newly cited.)

In regard to claims 1, 2, and 10, in figs. 1-4, Ohie discloses a first semiconductor chip 103, or LSI chip, a peripheral circuit area surrounding the central circuit area, and circuits being formed on the surface of the chip. See fig. 4, for example;

a second semiconductor chip 113 mounted on the central circuit area of the first chip;

a first electrode group 125 which is formed on an area between the central circuit and the peripheral areas of the first chip;

a second electrode group 105 which is formed on an outer area of the peripheral circuit area of the first chip;

a third electrode group 115 which is formed on the second chip;

a plurality of first wires 117 for electrically connecting the first electrode group and the third electrode group; and

external connection terminals on the element 9 which are electrically connected to the second electrode group through wires 107.

Ohie further discusses how circuits are formed on the chips, for example, in fig. 4. It should be noted that, electrical circuits and electronic elements are formed on the top surface of the first chip where all of the electrodes are formed. Ohie, however, does not expressly mention how digital and analog circuits are arranged on the surface of the chip.

It is common and obvious to one skilled in the art to arrange a circuit on the outside, or peripheral, area of the chip elements in this circuit can be used to regulate the voltage supply, for example, capacitors and resistor that are included in the circuit. For instance, Gutierrez, in figs. 2 and 3, discloses an analogous device having a high noise circuit and a low noise analog circuit, wherein the low noise circuit is formed on the peripheral area of the device. The low noise circuit further includes resistors and a ground plan which provide connection to the power supply. As mentioned above, this arrangement of the circuits provides a way to regulate the voltage supply, and it is common in the art.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time of the invention was made to arrange the circuit on a surface of a chip as taught by Gutierrez in order to regulate power supply from an external input.

In regard to claim 3, Ohie further discloses that the external terminals are conductive leads. See col. 6, lines 18-20.

In regard to claims 4, 11, 16, and 18, Ohie further discloses the size of the second chip is smaller than the first one, fig. 1, for example.

In regard to claim 5, Ohie further discloses that the chips are sealed with resin 10. See fig. 1 and col. 6, lines 23-25.

In regard to claims 6, 13, and 20, Ohie further discloses that:

the external terminals are conductive leads, mentioned above;

the leads are arranged a long the outer periphery of the first chip at positions separated from the other chip by a certain distance. See figs. 1 and 2;

the second group and the leads are electrically connected by second wires, mentioned above;

the first and second chips, and the wires are together sealed with resin, mentioned above, resin 10.

In regard to claim 7, Ohie further discloses that the first chip is formed on a support 8.

In regard to claim 8, Ohie's fig. 2 further shows the arrangement of the electrodes.

In regard to claim 9, Ohie further discloses the third group is formed along the outer area of the second chip, fig. 2.

In regard to claims 12, 17, and 19, as mentioned in claims 1 and 10 above, the analog circuit 316 is part of the low noise circuit. See Gutierrez's fig. 3.

In regard to claims 14 and 15, as mentioned above, Ohie discloses electrical connections include wires 107 and 117.

Response to Arguments

3. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

4. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nathan W. Ha whose telephone number is (571) 272-1707. The examiner can normally be reached on M-TH 8:00-7:00(EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nathan Ha
November 19, 2005

HOAI PHAM
PRIMARY EXAMINER